REMARKS

Claims 1-47 were pending at the time of the Office Action.

Claims 1, 2, 3, 5, 7, 13, 18, 21, 23, and 24 are amended.

No claims are added.

Accordingly, claims 1-47 are pending.

Applicant respectfully requests reconsideration and allowance of the subject application.

Objections to the Claims

Claims 2-3, 5, 6-10, 13-14, 18-33, and 41-47 are objected to for various informalities noted by the Examiner. Except as noted immediately below, the claims have been amended as suggested by the Examiner.

Several of the objections relate to recitation of various types of "logic". The Examiner suggests using the terminology "*a* . . . logic that . . .". For example, the Examiner suggests claim 8 be amended to recite "*a* calibration logic that sets . . .". It is respectfully submitted, however, that the suggested language is grammatically awkward and that the language as Original is grammatically correct. Accordingly, it is respectfully requested that these objections be withdrawn.

§ 112 Rejections

Claims 5 and 10 are rejected based on the Office's assertion that they recite functionality not described in the application. Specifically, the Office Action states that the specification does not teach how to derive a correction value.

Correction values, and how to determine them, are taught in the specification beginning at page 12. As stated there:

> The calibration logic 88 [Fig. 5] performs an initialization or calibration procedure to determine the appropriate correction values for the respective digital control values. The initialization procedure comprises varying digital control values PHASEA, PHASEB, PHASEC, and PHASED to produce a predetermined phase relationship between the clock signals. More specifically, the calibration logic varies digital control values PHASEA, PHASEB, PHASEC, and PHASED so that the buffered clock signals CLKA, CLKB, CLKC, and CLKD have approximately identical phases. The calibration logic then derives correction values from the digital control values PHASEA, PHASEB, PHASEC, and PHASED that produce such phase alignment. Generally, the correction values comprise the differences between the control values that produce phase alignment. Normally, one of the clock signals will be designated as a reference, and the differences will be calculated with respect to the control value corresponding to the reference.

Accordingly, the §112 rejection of claims 5 and 10 is unfounded. It is respectfully requested that these rejections be withdrawn.

Claims 23 and 24 are rejected based on the Office's assertion that recitation of "one or more delay elements" is indefinite. In particular, the Examiner states that "it is not understood how the delay elements delay the clock signal by a phase varying with PVT variations, wherein there is no connection between the delay elements and PVT variations compensated by the PVT-sensitive circuit taught in the disclosure of the application."

In response, it should be understood that the components from which the delay element is constructed are themselves subject to PVT variations—in many cases the same PVT variations as the recited PVT-sensitive circuit. Techniques are known in the art for making delay elements that vary with such PVT variations. Accordingly, the delay element can be made sensitive to its own PVT

variations, which can be assumed in many cases to at least approximate the PVT variations experienced by the recited PVT-sensitive circuit.

In response to the above, it is respectfully requested that all §112 rejections be withdrawn.

§ 102 Rejections

Claims 15-20 are rejected as being anticipated by the material described by the Applicant in the specification, in particular, by the circuit of Prior Art Fig. 2.

Claim 15 recites a method that includes "generating a plurality of clock signals in response to digital control values that specify desired relative phases . . .".

In addition, claim 15 recites "deriving correction values *from the digital control values* . . .".

In rejecting claim 15, the Examiner describes functionality of Fig. 2, but does not specify which signals in Fig. 2 are alleged to comprise correction values. Furthermore, the Examiner does not indicate how any such values are derived from digital control values. The rejection is invalid for this reason alone, in that the Examiner has made no correlation between the recited elements and the elements shown in the prior art figure.

Moreover, the circuit of Fig. 2 does not perform "deriving correction values *from the digital control values* . . .". Fig. 2 shows digital control values in the form of PHASE1 and PHASE2. However, it is clear from Fig. 2 that these control values are received only by the phase shifters 22 and 23. These phase shifters are not described as deriving correction values, and the Examiner has not pointed to

any such description or operation. Claim 15 is allowable for this additional reason.

Claim 18, similarly, recites that "the calibration logic derives one or more correction values from the digital control values that produce the predetermined phase relationship . . .". As discussed above, Fig. 2 and its related discussion do not disclose this characteristic.

Accordingly, it is respectfully requested that the rejection of claims 15 and 18 be withdrawn.

Claims 16, 17, 19, and 20 depend from either claim 15 or claim 18, and are thus allowable by virtue of their dependence on allowable base claims.

It is respectfully requested that the rejections of claims 15-20 be withdrawn.

§ 103 Rejections

Claims 1, 3-4, 6, 8-9, 11-14, and 25-47 are rejected as being obvious over Applicant's Fig. 2 in view of US Patent No. 5,479,457 to Waters.

Fig. 2 shows clock generation circuits 22 and 23 that generate clock signals CLK1 and CLK2 having phases that are specified by digital phase control values PHASE1 and PHASE2 (see specification beginning at page 1, line 25).

Waters shows a circuit (Fig. 4) in which a relative phase is measured by comparing outputs of counters. The counters are clocked by clock signals to produce digital outputs that represent relative phases of the clock signals. Note that the digital outputs are *derived from* the clock signals. They do not control or establish any phases.

Claim 1 recites a first digital control value "establishing the phase of a first clock signal", and a second digital control value "establishing the phase of a

second clock signal." In addition, claim 1 recites "comparing the first and second digital control values . . .."

Fig. 2 shows first and second digital control values PHASE1 and PHASE2. However, Fig. 2 does not compare the digital control values. Rather, the circuit of Fig. 2 compares the clock signals that are produced in response to the digital control values.

The Office Action apparently concedes that Fig. 2 does not compare digital control values, instead asserting that this would have been obvious in light of Waters. However, the Waters circuit does the same thing as Fig. 2: it compares the clock signals themselves, rather than the digital control values that establish the phases of the clock signals.

Although Waters uses digital phase values in his comparison, the digital phase values do not satisfy the recited elements in claim 1 of "establishing the phase" of the first or second clock signal. Rather, the digital phase values are *derived* from the clock signals themselves in order to perform the comparison. The compared digital phase values are not *control* values and do not *establish* any clock phases. Accordingly, they do not satisfy the elements of claim 1.

If Waters were used in combination with the circuit shown in Fig. 2, it would not result in the claimed relationship of elements. Specifically, there is nothing in Waters that would suggest comparing values (digital or otherwise) that *control* the phases of the clocks, as opposed to his preferred and disclosed method of comparing values that have been *derived from* the clock signals. Indeed, Waters does not even show any phase control values, or any way to control phases.

Therefore, even the combination of Fig. 2 and Waters does not render claim 1 obvious. Accordingly, the rejection of claim 1 should be withdrawn.

Claim 6, similarly, recites first and second digital control values that establish phases of clock signals, and "phase detection logic that compares the first and second digital control values . . .". As already discussed, neither Fig. 2 nor Waters shows or suggests comparing *control* values. Accordingly, claim 6 should be allowed.

Claims 11 and 13 recite a "measurement clock signal having a phase that is established . . . by a phase control value." Claims 11 and 13 further recite "evaluating" the phase control value. Again, nothing in Fig. 2 or in Waters even remotely suggests performing any sort of evaluation on a phase control value. Waters does not even show a phase control value.

Claim 25 recites an "input timing signal having a phase that is established . . . by an input phase control value", and "evaluating the input phase control value . . .". Claim 25 is rejected using the same rationale as the claims above. However, as already discussed, nothing in either Fig. 2 or Waters suggests any sort of evaluation of a phase control value. Accordingly, the rejection of claim 25 should be withdrawn.

Claim 34 recites "setting a target phase control value to establish the phase of the target clock signal" and "setting an input phase control value to establish the phase of an input clock signal". Claim 34 further recites "comparing the target phase control value and the input phase control value . . .". Again, nothing in the cited prior art suggests evaluating or comparing phase control values, for any purpose. The rejection of claim 34 should therefore be withdrawn.

Claim 41 recites an "input phase control value that establishes the calibrated phase of [an] input clock signal," and "evaluation logic that evaluates the input phase control value . . .." As already discussed, Fig. 2 does not perform any evaluation of any phase control value, and Waters does not even show any phase control value. Claim 41 should therefore be allowed.

Claims 2-5, 7-10, 12, 14,26-33, 35-40, and 42-47 all depend from one of the base claims discussed above, and are allowable for that reason as well as for the additional elements they recite that are not suggested by the cited prior art.

Claims 21-24 are rejected as being obvious over the Applicant's Fig. 2 in view of US Patent No. 5,859,550 to Brandt. Brandt is apparently cited for its disclosure of a PVT-sensitive circuit.

Claim 21 recites "varying the phase control value to find a PVT . . . adjustment value that produces a predetermined phase relationship between the delayed measurement clock signal and the reference clock signal." The Examiner apparently relies on Fig. 2 as showing this step, but fails to provide any specifics. Brandt is cited only for its discussion of a PVT circuit and clearly does not show or suggest a "varying" step as recited in claim 21.

It is respectfully submitted that Fig. 2 and its related discussion do not suggest this step.

Furthermore, even if Fig. 2 could somehow be construed as producing an adjustment value, the Applicant can find nothing that would suggest adjusting a circuit based on value determined in this fashion.

Accordingly, it is believed that the §103 rejection of claim 21 is without merit, and should be withdrawn.

Claim 23 similarly recites "calibration logic that varies the phase control value to find a PVT adjustment value that produces a predetermined phase relationship between the delayed measurement clock signal and the reference clock signal." As discussed with respect to claim 21, neither Fig. 2 nor Brandt discloses this step.

Claims 22 and 24 depend from claims 21 and 23, respectively, and are allowable and for that reason as well as for the additional elements they recite that are not suggested by the cited prior art.

Conclusion

Reconsideration and allowance of all claims is respectfully requested.

Respectfully Submitted,

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